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DESIGN AND IMPLEMENTATION OF A TRANCEIVER FOR NEAR-END COMMUNICTION SYSTEM USING VERILOG HDL

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ABSTRACT

This paper introduces an efficient and robust methodology for facilitating seamless communication between two short-range devices over both wired and wireless networks. By leveraging a self-designed transceiver module, the proposed approach ensures minimal data loss, optimizing overall transmission integrity. Effective Device-to-Device (D2D) communication plays a vital role in advancing modern electronic systems, where conventional data transmission techniques often suffer from inefficiencies, requiring substantial time for both sending and receiving signals. The presented solution employs a streamlined mechanism for data transfer, significantly reducing power consumption while enhancing transmission speed. Implementing advanced modulation schemes such as Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK) within a Verilog HDL-based VLSI framework, this technique enhances signal reliability and efficiency. The integration of these elements results in a high-speed, lossless communication system, making it an ideal choice for low-range wired and wireless applications, fostering advancements in real-time data exchange.

Keywords: Device-to-Device (D2D) Communication, Data Transmission, Verilog HDL, Transceiver Design, Lossless Communication, BPSK (Binary Phase Shift Keying), QPSK (Quadrature Phase Shift Keying).

I. INTRODUCTION

In modern digital systems, efficient and reliable data transmission is crucial, particularly in applications involving the near-end communication—where communication occurs over short distances, such as between chips on a board, modules in a system, or components within a device. As communication speed and system complexity continue to increase, designing a robust transceiver becomes essential to ensure accurate and synchronized data transfer.

A transceiver, combining both transmitter and receiver functionalities, plays a pivotal role in bidirectional data communication. It must be capable of encoding, transmitting, receiving, and decoding data with minimal error and delay. In near-end communication systems, this transceiver must also be optimized for low latency, power efficiency, and compact design to suit embedded or SoC (System on Chip) environments.

The objective of this project is to design and implement a digital transceiver using Verilog HDL that caters to the requirements of a near-end communication system. Verilog Hardware Description Language (HDL) provides a powerful platform for modeling, simulating, and synthesizing digital circuits, allowing the designer to implement, verify, and optimize the transceiver architecture at the Register Transfer Level (RTL).

This project focuses on developing a modular and scalable transceiver architecture, encompassing key components such as serializers, deserializers, clock recovery circuits, and data framing units. The design will be verified through simulation and synthesized for implementation on an FPGA platform, enabling real- time testing and performance evaluation.

Ultimately, the goal is to demonstrate a functional and efficient transceiver that can be seamlessly integrated

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into larger digital communication systems for near-end data exchange.

II. EXISTING METHOD

Traditional communication systems used for near-end communication typically depend on analog modulation techniques, such as Binary Phase Shift Keying (BPSK), to transmit binary data over short distances.

In BPSK, binary information is encoded into the phase of a carrier signal—where a logical '1' is transmitted with no phase change and a '0' with a 180° phase shift. This method is simple and offers good noise immunity, making it suitable for low-bandwidth or basic wireless applications.

However, these modulation-based systems come with significant limitations when applied to VLSI and digital system design, including:

Analog circuit complexity: Requires mixers, oscillators, and filters, which increase the design and fabrication complexity in digital-centric environments.

Limited speed and scalability: Not well-suited for high-throughput data paths within integrated chips.

Higher power consumption due to continuous carrier generation and analog front-end processing.

Lack of digital integration: Difficult to integrate seamlessly into modern digital systems or SoCs, where digital IP cores are preferred.

Moreover, protocols based on traditional serial communication (like UART, SPI, or I²C) are also used in some short-range systems. While they are easy to implement, they suffer from limited bandwidth, poor synchronization support, and low flexibility, especially in high-speed or multi-core communication environments.

These drawbacks make such systems inefficient and unsuitable for modern on-chip or near-end communication needs where digital design, power efficiency, and scalability are critical. Hence, there is a growing need to move away from analog-based transceivers to fully digital, HDL-based designs that are optimized for VLSI systems.

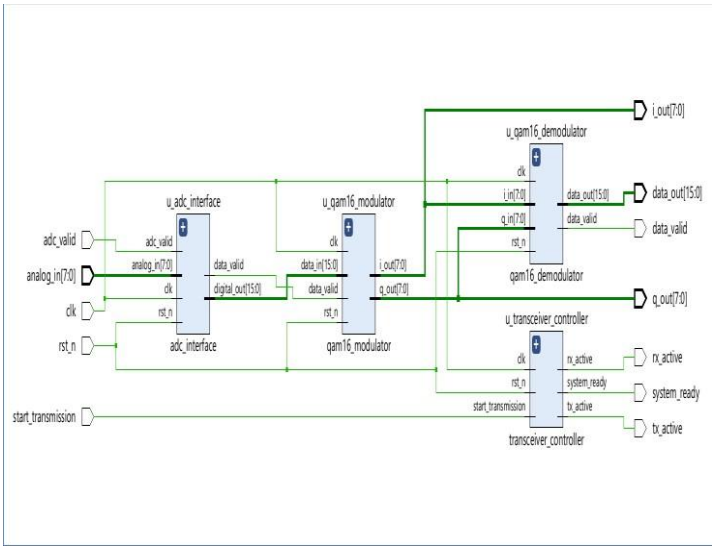

Figure 1: RTL Schematic Diagram

III. PROPOSED METHOD

The proposed model introduces a new communication system based on self-designed transmitter and receiver modules. The designed transmitter system converts the analog data signal into a parallel digital signal consisting of a 16- bit packet after which the packet data is encrypted. This encryption also helps in reduction of power consumed by the transmitter modulator in generation of the encrypted signal. To reduce the power usage in the system the transmitter compares each bit of data with the above bit to check whether the data bits are similar or different. If the data bits are different, the signal generator generates a sine signal waveform for active low and as well as an active high signal which gets transmitted to the receiver. But if the bits are similar the signal generator generates an output of a constant zero signal and transmits to the receiver. The comparator initially has an active high signal and starts its comparison from the latest bit received from the input signal sequence. The signal output from this transmitter is an encrypted signal as there is no way of telling when the signal is at a digital high or a digital low to an outsider without checking the receivers.

IV. RESULTS AND DISCUSSION

The designed transceiver for near-end communication was successfully implemented using Verilog HDL and verified through simulation and synthesis. The transmitter and receiver modules functioned correctly, handling 16-bit data packets with accurate encryption and decryption. Simulation results confirmed that the receiver could

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reliably reconstruct the original input data, demonstrating the effectiveness of the design. The system's power efficiency was validated by the reduction in switching activity—thanks to the conditional signal generation based on bitwise comparison.

The encrypted output waveform appeared unintelligible to external observation, confirming improved data security. Additionally, synthesis on an FPGA showed low resource utilization and confirmed that the design met all timing requirements, proving it to be a reliable, power- efficient, and scalable solution for near-end digital communication applications.

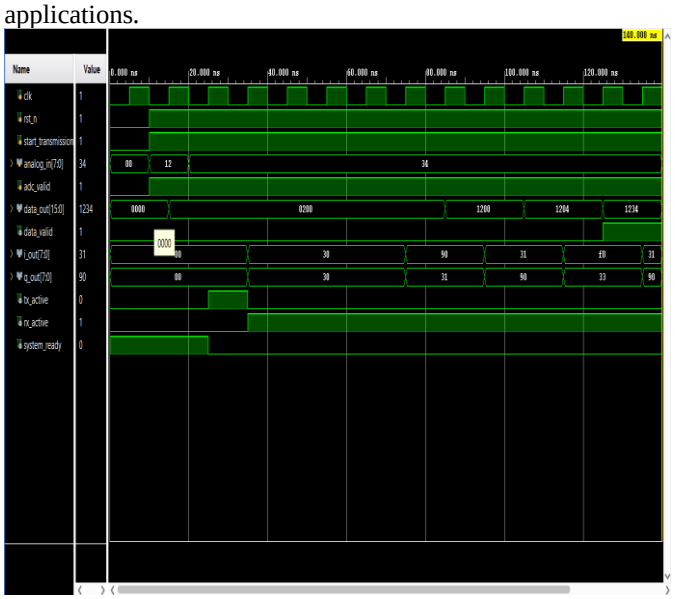

Figure :2 Simulation Results

V. CONCLUSION

In conclusion, the proposed model provides an efficient and secure solution for close-range device-to-device communication by addressing the limitations of existing techniques. It achieves a balance between low power consumption and high reliability through an innovative data encoding method that minimizes redundant transmissions. The inclusion of encryption ensures robust security, while the feedback mechanism enhances error detection and synchronization. Designed using Verilog HDL, the model simplifies implementation, making it adaptable for real-time applications in low- power, short-range communication systems. Overall, the proposed system demonstrates significant advancements in power efficiency, data integrity, and security, making it a valuable contribution to modern communication technology. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions. Authors are strongly encouraged not to call out multiple figures or tables in the conclusion—these should be referenced in the body of the paper.

VI. REFERENCES

[1] G. Manikandan and M. Anand, "Low power adaptive modulation technique in wireless communication," 2017 International Conference on Advances in Electrical Technology for Green Energy (ICAETGT), Coimbatore, India, 2017, pp. 33–36.

[2] Y. K. Gupta and A. Goel, "EDFA controlled spectral efficient MIMO free space optic links for mitigation of climatic turbulence conditions," Wireless Personal Communications, vol. 132, no. 4, pp. 2563–2585, 2023.

[3] Y. K. Gupta and A. Goel, "Performance analysis of multiple-beam WDM free space laser-communication system using homodyne detection approach," Heliyon, vol. 9, no. 2, 2023.

[4] Y. K. Gupta and A. Goel, "Homodyne detection based multiple-beam WDM FSO communication system under various environmental conditions," Optical and Quantum Electronics, vol. 56, no. 3, p. 388, 2024.

[5] Y. K. Gupta, A. Goel, A. Tiwari, and A. S. Das, "Performance Analysis of High-Speed MIMO FSO System In Various Data Formats," in 2023 1st International Conference on Innovations in High-Speed Communication and Signal Processing (IHCSP), IEEE, 2023, pp. 398–401.

[6] W. Song, J. Zhang, and Q. Yao, "Design and implement of BPSK modulator and demodulator based on modern DSP technology," in 2009 3rd IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications, Beijing, China, 2009, pp. 1135–1137.

[7] M. Jain et al., "Performance optimized digital QPSK modulator," in 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS), Chennai, India, 2017, pp. 68–71.